CLAIMS

We claim:

1. An apparatus, comprising:

a register having a plurality of bit locations to store data;

a demultiplexer circuit coupled to the register to direct a bit of incoming data to a selected bit location in the register;

a write pointer circuit coupled to the demultiplexer circuit to provide a write pointer address for the selected bit location to the demultiplexer circuit, being responsive to a strobe signal to adjust the value of the write pointer address; and being responsive to an input signal to set the write pointer address to a predetermined value; and

a multiplexer circuit coupled to the register and to the write pointer circuit to provide a data output, the data output being at least one of a selected bit location in the register or a selected bit of the write pointer address.

2. The apparatus of claim 1 wherein the write pointer circuit is response to the input signal to reset the write pointer address.

3. The apparatus of claim 1 wherein the register is responsive to the strobe signal to store the data in the bit location specified by the write pointer address.

4. An apparatus, comprising:

a register having a plurality of bit locations to store data;

a demultiplexer circuit coupled to the register to direct a bit of incoming data to a selected bit location in the register;

a write pointer circuit coupled to the demultiplexer circuit to provide a write pointer address for the selected bit location to the demultiplexer circuit, being responsive to a strobe signal to adjust the value of the write pointer address; and being responsive to an input signal to set the write pointer address to a predetermined value; and

a multiplexer circuit coupled to the register and to the write pointer circuit to provide a data output, the data output being at least one of a selected bit location in the register or a selected bit of the write pointer address.

a memory controller coupled to the multiplexer and to the write pointer circuit to cause the multiplexer circuit to select at least one bit of the write pointer address, to determine the write pointer address, and to provide the input signal to set the write pointer address to a predetermined value.

5. The apparatus of claim 4 wherein the write pointer circuit is response to the input signal to reset the write pointer address.

6. The apparatus of claim 4 wherein the register is responsive to the strobe signal to store the data in the bit location specified by the write pointer address.